# 4 Design

## 4.1 Design Content

The design content of our project includes designing an efficient approach to implement a video compression and decompression algorithm on the Zynq 7000 FPGA. This requires having clear hardware designs/schematics that portray the functionality of the video pipeline on the FPGA.

## 4.2 Design Complexity

The design of a video compression system involves creating custom hardware and custom software, and requires them to cohesively work together along with given IP circuits that we must also choose. We must design video compression algorithms that work extremely fast, and have it interface with its associated hardware that we've designed. The hardware that we design will be very complex due to the nature of video compression and decompression. Hardware designs also take into account all the limitations and constraints that are ignored in software design.

## 4.3 Modern Engineering Tools

Python will be used for the software side for video compression and decompression just to test algorithms. We will then have to write C code that does video compression. Some aspects of the video compression will be done in hardware, which at the easiest, requires the code to be designed in C and an API used to convert to hardware, and at the hardest, requires Verilog to be written for the hardware. Draw.io is a tool that will be used for drawing schematics and block level diagrams.
HARDWARE TOOLS HERE (if any were missed)

## 4.4 Design Context

| Area | Description | Examples |
|---|---|---|
| Public health, safety, and welfare | This project can potentially indirectly affect the safety or well-being of a John Deere customer in the future since the video compression/decompression can be used for videos running on vehicle displays. | Having lossy images/videos in a tractor/sprayer/etc. can provide a major risk of the vehicle malfunctioning. |
| Global, cultural, and social | This project could have applications in increasing crop yield for tractors. This project should decrease the cost of hardware inside tractors, allowing farmers to save money when they have to buy new tractors. This would lead to a reduction in the cost of food and crops. | An efficient implementation will satisfy the client and potential customer's aim of having a cheaper and more advanced solution. |

| | | |
|---|---|---|
| Environmental | Having our client as John Deere may help illustrate the kind of environmental impact our project may have. Since tractors aren't fully electric, they do pollute, but the idea of our project is to help tractors run more efficiently, therefore reducing the time of use. | Our project being in the realm of precision farming means that as an engineer, we are trying to innovate the way tractors are traditionally operated, such that the added use of software, and hardware is able to automate tasks, increase yield, and decrease time allotted to various tasks. |
| Economic | This project will save money for both John Deere and farmers spending money on new tractors. This equipment might interface with technology that increases crop yield, and increases autonomy. This saves farmers money, increases supply on crops, and thus decreases the price of crops. | Our solution being implemented on an FPGA leads to a decrease in cost for John Deere since it'll be faster than a fully software approach and will off-load from the CPU. This results in freeing up more space on the CPU for other tasks. |

## 4.5 Prior Work/Solutions

There exists dedicated hardware video compression chips. These however, are mainly only found on GPU's, which require a lot of power, are expensive, and they are not dedicated to one singular task like our hardware will be. There also exists video compression algorithms and encoders like H265. Video compression techniques are also a thoroughly researched topic.

## 4.6 Design Decisions

We've kept in mind complexity and cost when designing the layout of the hardware. We've also decided we will use the Zybo Z7-10 as our dev-board because it has both HDMI-in and HDMI-out. We've chosen to use VDMA in and out, Memory buffer as storage, CPU to interface with the hardware and possibly do some software compression with. We will also have our own custom hardware designs. We've chosen to have a CPU so that we can send information to memory, and we can interact with the hardware if needed, and so future engineers can interface with the CPU to receive the information to do other things with.

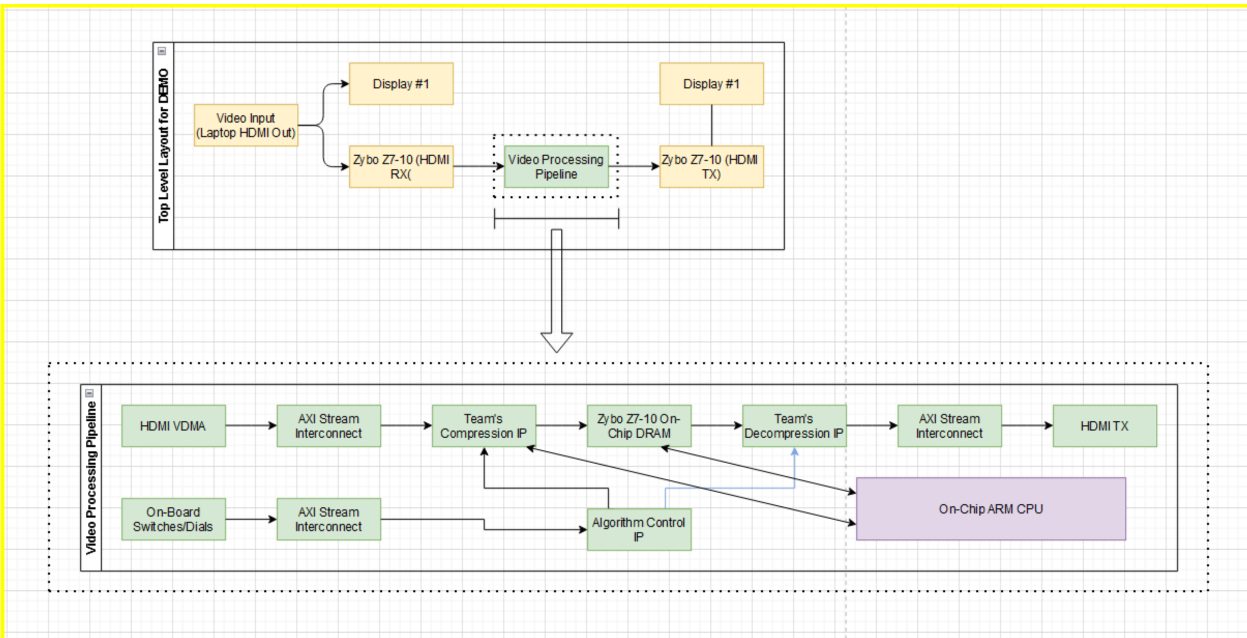
## 4.7 Proposed Design

We've created a basic hardware diagram for how we want to lay out and arrange the components of our hardware. We've researched compression algorithms and techniques to be considered for implementation in hardware. We've gathered dev-boards to be used for testing and implementation.

### 4.7.1 Design 0 (Initial Design)

#### Design Visual and Description

The Zybo Z7-10 converts the data on its HDMI RX line to allow for HDMI VDMA. This is how we will be accessing the HDMI data to run compression on. Once we have the VDMA data, we can compress it and send it to memory provided by the on-board DRAM. Once in memory, here is where we can leverage use of the on-board ARM processor to gather details on latency, compression ratio, memory savings, and loss amount for the algorithm. The Memory will store a compressed frame of the video to be accessed by other hardware and software out of the scope of this project. Then the compressed data will be taken out of memory and decompressed to provide a video. Another goal that we have is to view the tradeoffs between speed vs compression ratio vs video quality by allowing these metrics to be adjusted with some sort of dial or switch control interface. The first design states that we will be using the on-board slide switches but in the future, a separate dial peripheral could be added.




#### Functionality

Our design is intended to operate on John Deere equipment to minimize on device storage. All of the cameras on a tractor, sprayer, planter, combine harvester will need to have their video compressed with near-zero latency so that they do not require huge amounts of memory. The current design will hypothetically have near-zero latency and output lossless or near-lossless video after decompression thus satisfying the functional requirements. the hardware will temporarily keep the compressed video data in memory for future use.

**NOTE: The following sections will be included in your final design document but do not need to be completed for the current assignment. They are included for your reference. If you have ideas for these sections, they can also be discussed with your TA and/or faculty adviser.**

#### 4.7.2 Design 1 (Design Iteration)

*Include another most matured design iteration details. Describe what led to this iteration and what are the major changes that were needed in Design 0.*

### Design Visual and Description

Include a visual depiction of this design as well highlighting changes from Design 0. Describe these changes in detail. Justify them with respect to requirements.

### 4.8 Technology Considerations

*Highlight the strengths, weakness, and trade-offs made in technology available.*

*Discuss possible solutions and design alternatives*

### 4.9 Design Analysis

- *Did your proposed design from 4.7 work? Why or why not?*
- *What are your observations, thoughts, and ideas to modify or iterate further over the design?*