EE/CprE/SE 492 WEEKLY REPORT 3

2/10/24 – 2/24/24

Group number: 12

Project title: Pipelined Video Compression & Decompression on FPGA

Client &/Advisor: John Deere & Joseph Zambreno

Team Members/Role: Colsen Selk - Software, Kareem Eljaam - Hardware, Caleb Rock - Hardware, Benjamin Meinders - Software, Logan McDermott - Hardware

- **Weekly Summary**

Software - We finished implementing LZW in Java and were getting ready to convert it over to C, then realized that this is not going to work well for our project as the data for high def images are not repetitive enough. Going forward, we are looking into better algorithms for the project, or IPs for the block design.

Hardware - We successfully have an HDMI passthrough working and can use our generated bitstream as a hardware platform for a Vitis project. We experimented with removing unnecessary IP blocks from the Demo for our project and were successfully able to remove unnecessary blocks while maintaining the passthrough functionality. We also spent time trying to obtain a License for IP blocks from AMD and are working towards porting these new modules into our project.

- **Past week accomplishments** *(Please describe/summarize as to what was done, by whom, when and, collectively as a group. This should be about a paragraph or two in length. Bulleted points are acceptable as well. Please keep only your technical details related to your project. Figures, schematics, flow diagrams, pseudocode, and project related results are acceptable, but please ensure that they are legible (clear enough to read) and to provide an explanation. If researching a topic, please add a few details about what was learned and how it is relevant to the project. If two or more people worked on a single task, be sure to distinguish how each member contributed to the task. Specific details relating to the assistance provided to other members may be included here.* ***Do not include classwork, such as individual reflection assignments, and group***

meetings as part of your duties.)

- Caleb: Got HDMI pass through running on hardware. Worked on getting IP cores implemented into block design.
- Logan: Researched licensing for useful IP blocks and worked with Caleb and Kareem to get the hardware bitstreams to properly generate after removing unnecessary IP blocks. Also attempted to port in IP blocks provided by Dr. Zambreno but have not been successful yet.
- Kareem: Did some experimenting with the HDMI passthrough block design while working with Caleb and Logan. Integrated the AXIS passthrough IP core into the design but ended up not getting a video stream. I also contacted our client to update him on where we're at.
- Ben: Got LZW compression/decompression implemented in Java. Started researching other compression algorithms that will work better for our project.
- Colsen: Started researching other compression algorithms that will work better for our project (BWT). found Python implementation for BWT to be tested

- **Pending issues** *(If applicable: Were there any unexpected complications? Please elaborate.)*
  - We have found some potentially helpful IP cores to use but are struggling to figure out how to actually implement them into the block design.
  - The chosen compression algorithm may not work well with the type of data that the camera may be providing.
  - The demo project we are using as a template is in Verilog when we were expecting to work in VHDL

- **Individual contributions** *(Creating this section is optional, but it is* ***Required to include the "Hours Worked for the Week" and their "Total Cumulative Hours" for the project for each member somewhere relevant in your report. Your individual weekly hours should be at a minimum of 6-8 hours for this course. So please manage your time well. Also, ensure that individual contributions support your claim to the weekly hours. Be honest with the reports.****)*

NAME	**Individual Contributions** *(Quick list of contributions. This should be short.)*	**Hours this week**	**HOURS cumulative**
Colsen Selk	BWT Testing	6	16
Logan McDermott	Hardware passthrough. IP troubleshooting	6	13
Caleb Rock	Hardware passthrough. IP troubleshooting	7	20
Ben Meinders	LZW implemented. Algorithm research.	6	20
Kareem Eljaam	Hardware passthrough. IP troubleshooting	6	13

- **Plans for the upcoming week** *(Please describe duties for the upcoming week for each member. What is(are) the task(s)?, Who will contribute to it? Be as concise as possible.)*

  - Caleb: Keep working with Logan and Kareem and potentially the faculty advisor to successfully implement the IP cores into the block design.
  - Logan: Discuss our sticking points with Dr. Zambreno
  - Kareem: Plan meeting with client, and continue to work with Logan and Caleb to get the AXIS passthrough IP core working.
  - Ben: Discuss what the next steps for compression may look like and do research on video overlays.
  - Colsen: Convey how LZW works, work on BWT implementation

- **Broader Contexts**

((1) updates to broader context effects, (2) plans to demonstrate evidence of positive effects, and (3) ways to address or justify negative effects based on meetings with your team, client(s), and advisor.)

To start off, since we have the HDMI passthrough working and are actively getting help from our faculty advisor, we need to set up a meeting with our client to make sure we can compare and contrast our progress to ensure that we are on the same page with project progress. The HDMI passthrough is something we can show as tangible

progress, and we also have LZW implemented to show if needed. The negative aspect of this is that the LZW implementation isn't compressing and is actually enlarging a files size. Something that we need to accomplish in the immediate future is asking what kind of camera is going to be used, and how the data will be transmitted so we can pick an algorithm/find an IP that will handle this project more efficiently. We also need to confront issues caused by Verilog/VHDL mismatch and see if the advisor provided IP cores can be ported to VHDL.